

WHAT IS CLAIMED IS:

1. A processor system comprising:  
a central processing unit;  
a writeable memory;  
5 means for external communication;  
operation mode selection means for selecting an  
operation mode;  
control means for stopping the operation of said  
central processing unit and writing to said memory an  
10 IPL program transferred from the outside through said  
communication means when an IPL operation mode is  
selected by said operation mode selection means, and  
for thereafter canceling the stoppage of the operation  
of said central processing unit; and  
15 IPL operation means for executing the IPL program  
written to said memory through the operation of said  
central processing unit to download a system program.
2. A processor system according to claim 1,  
20 wherein said control means includes:  
mapping control means for mapping said writeable  
memory to an area including an address which said  
central processing unit first reads immediately after  
startup in the IPL operation mode; and  
25 write control means for controlling writing of the  
IPL program such that the writing starts from the  
address read first.

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3. A processor system according to claim 1,  
wherein said control means includes:

detection means for detecting a situation where  
transfer of the IPL program should be terminated; and

5 termination processing means for terminating  
writing to said memory when a situation where the  
transfer should be terminated is detected by said  
detection means.

10 4. A processor system according to claim 3,  
wherein said detection means detects a situation where  
the transfer should be terminated by ascertaining that  
a transferred data amount set in advance has been  
reached.

15 5. A processor system according to claim 3,  
wherein said detection means detects a situation where  
the transfer should be terminated by detecting from  
transferred data a code designating termination of  
20 transfer.

6. A processor system according to claim 1,  
wherein said control means includes bus control means  
for changing a connection of a bus according to the  
25 operation mode, and the bus control means changes the  
memory as an IPL program writing destination according  
to the operation mode.

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7. A processor system according to claim 1,  
wherein said control means performs control such that a  
check program for checking the operation or condition  
of a certain device is written to said memory together  
5 with the IPL program, and the check program is executed  
when said central processing unit starts operating.

8. A processor system according to claim 7,  
wherein the check program is a program for checking the  
10 operation of a peripheral device connected to the  
processor system.

9. A processor system according to claim 7,  
wherein the check program is a program for checking the  
15 state of a memory connected to the processor system.

10. A processor system according to claim 7,  
wherein the check program is a program for checking the  
state of connection of a peripheral device connected to  
20 the processor system.

11. A method of starting a processor system  
having a central processing unit, a writeable memory,  
and a communication portion for external communication,  
25 said method comprising the steps of:

stopping the operation of said central processing  
unit when an IPL operation mode is selected;

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writing to said memory an IPL program transferred from the outside through said communication portion;

canceling the stoppage of the operation of said central processing unit after said writing; and

5       executing the IPL program written to said memory through the operation of said central processing unit to download a system program.

10       12. A method according to claim 11, wherein said writeable memory is mapped to an area including an address which said central processing unit first reads immediately after startup in the IPL operation mode, and said writing of the IPL program is controlled so as to start from the address read first.

15       13. A method according to claim 11, wherein a situation where transfer of the IPL program should be terminated is detected, and said writing to said memory is terminated when a situation where the transfer  
20       should be terminated is detected.

25       14. A method according to claim 13, wherein a situation where the transfer should be terminated is detected by ascertaining that a transferred data amount set in advance has been reached.

15. A method according to claim 13, wherein a situation where the transfer should be terminated is

0970308-012901  
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detected by detecting from transferred data a code designating termination of transfer.

16. A method according to claim 11, wherein the  
5 memory used as an IPL program writing destination is changed according to the operation mode by changing a connection of a bus according to the operation mode.

17. A method according to Claim 11, wherein  
10 control is performed such that a check program for checking the operation or condition of a certain device is written to said memory together with the IPL program, and the check program is executed when said central processing unit starts operating.

18. A method according to claim 17, wherein the  
15 check program is a program for checking the operation of a peripheral device connected to the processor system.

19. A method according to claim 17, wherein the  
20 check program is a program for checking the state of a memory connected to the processor system.

20. A method according to claim 17, wherein the  
25 check program is a program for checking the state of connection of a peripheral device connected to the processor system.

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